AMENDMENTS TO THE DRAWINGS

The attached eight sheets of formal drawings the original informal sheets of drawings

Attachment: Replacement Sheets

REMARKS

Reconsideration and allowance are requested.

The abstract is amended and is now less than 150 words. Withdrawal of the objection to the abstract is requested.

Formal drawings are submitted with this amendment. Withdrawal of the objection to the drawings is requested.

Claims 1-22 stand rejected under 35 U.S.C. §102 for anticipation based on Chen. This rejection is respectfully traversed.

To establish that a claim is anticipated, the Examiner must point out where each and every limitation in the claim is found in a single prior art reference. *Scripps Clinic & Research Found. v. Genentec, Inc.*, 927 F.2d 1565 (Fed. Cir. 1991). Every limitation contained in the claims must be present in the reference, and if even one limitation is missing from the reference, then it does not anticipate the claim. *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565 (Fed. Cir. 1986). Chen fails to satisfy this rigorous standard.

The claims relate to performing more quickly an absolute difference calculation on portions of first and second data elements in a data processing apparatus. Quicker calculation is particularly advantageous in the light of the ever shorter clock cycles being implemented in contemporary data processing apparatuses.

Chen describes a floating-point calculation apparatus. A difference between exponent values and an inverted value thereof is calculated using a subtractor. One of the difference and the inverted difference values is selected in accordance with a signal indicating which of the exponent values is greater. Because only one subtractor is used, reduced circuit scale, chip real estate, and power consumption can be achieved.

The Examiner's comparison of the features of claim 1 with Chen centers around Figure 7 of Chen. The Examiner equates the "comparison logic" with item 202 and the "absolute difference logic" with items 201, 103 and 104. However, claim 1 further defines the absolute difference logic, and here, the Examiner's comparison breaks down. Specifically, claim 1 recites that the absolute difference logic comprises "adder logic configured to invert one of said portions to produce an inverted data element portion and to add the inverted data element portion to the other of said portions and to the comparison result received from the comparison logic in order to produce an intermediate result."

For the "adder logic configured to invert one of said portions to produce an inverted data element portion," the Examiner points to Figures 4 and 8, which respectively illustrate the structure of the 2's complement subtractor 101 of Figure 2 and the structure of the 1's complement subtractor 201 of Figure 7. But claim 1 defines the adder logic as being configured to "add the inverted data element portion to the other of said portions *and to the comparison result received from the comparison logic.*" Although "/IB" may be considered the "inverted data element portion" and "IA" as the "other of said portions," it is not correct to contend that Chen's subtractor 101/201 adds to the sum of IA and /IB "the comparison result received from the comparison logic." Recall that the Examiner equates the "comparison logic" with item 202 of Figure 7. The "adder logic" 201 illustrated in Figures 4 and 8 does not receive the comparison result from the comparison logic. Instead, as is clear from Figures 4 and 8, the C_{in} input is hardwired to either "1" or "0", respectively, depending on the embodiment (i.e., 2's complement subtractor 101 or 1's complement subtractor 201). In addition, *the output of the comparison logic 202 is never used as part of an addition sum* in Chen; instead, the comparison output controls or "steers" the multiplexer 104 and right-shifter 108.

Chen's multiplexer 104 cannot form part of the Examiner's interpretation of the "adder logic" of claim 1, since the claimed adder logic "[produces] an intermediate result," which is then operated on by the "output logic," defined in the final paragraph of claim 1. To the contrary, the Examiner equates the output logic of claim 1 with the inverter 103 and multiplexer 104 of Figures 2 and 7 in Chen.

Chen is also deficient with respect to another feature recited in the final sub-paragraph of claim 1 that defines the "output logic operable to generate an inverted version of the intermediate result...." In the embodiments in Chen illustrated by Figures 2 and 7, one of the inputs into multiplexer 104 is always an approximation – the inverted input "≈(EB-EA)" in Figure 2 and the uninverted input "≈(EA-EB)" in Figure 7. See column 9, lines 12-40 and column 11, lines 45 to column 12, line 3, respectively. As a result, Chen must correct for the approximation using the output of compensating shift circuit 108. See column 9, lines 46-50 and column 12, lines 12-16 respectively. Consequently, Chen does not (and cannot) disclose "[outputting] as the absolute difference either the intermediate result or the inverted version of the intermediate result," as recited in claim 1, because the absolute difference output by multiplexer 104 requires additional correction for one of the inputs.

In contrast, the "adder logic configured to invert one of said portions to produce an inverted data element portion and to add the inverted data element portion to the other of said portions and to the comparison result received from the comparison logic in order to produce an intermediate result" permits the true result of the absolute difference to be generated (this distinction is described in further detail below).

Lacking multiple features from independent apparatus claim 1 and analogous features in independent method claim 12, Chen fails to anticipate claims 1-22. Indeed, Chen can only

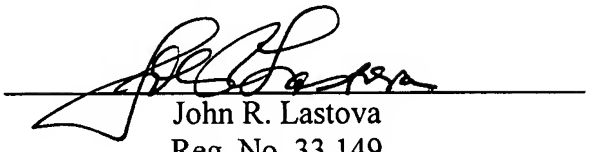
perform an approximate absolute difference between a portion of a first data element and a portion of a second data element (prior to correcting for the approximation later on). So there is a need for an improved calculation technique that eliminates such a need for later correction. The structure of claim 1 meets that need using a simple but effective mechanism for determining an absolute difference of data element portions A and B irrespective of whether A>B or B>A. Although useful for obtaining an absolute difference between any two data element portions, that structure provides particular benefit in the non-limiting context of determining an absolute difference of two floating point significands.

If the significand processing in Chen is considered, it can be seen that the significands FA and FB are routed via a swap unit 20 before being forwarded to adder/subtractor 8. In particular, the exponent difference calculator 15 steers the swap unit 20, which itself takes the significand portions FA and FB as its inputs. The use of such a swap unit is an example of the approach discussed in page 2, lines 3-10, and page 16, lines 10 to 18 of the present application. As stated there, as cycle times decrease, such a swap operation becomes less and less manageable. Chen hopes to reduce the scale of the circuit and "chip real estate" (see abstract) rather than improve speed as the inventors in this case did. The example in Figure 1 of the present application shows how improved speed is achieved because there is no need for any swap unit prior to the input to adder 80.

The application is in condition for allowance. An early notice to that effect is requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 
John R. Lastova
Reg. No. 33,149

JRL:maa
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100